

## 48451 ADVANCED DIGITAL SYSTEMS

<b>Course Name(s):</b>	Bachelor of Eng. - Diploma of Eng. Practice Bachelor of Eng. - Grad. Cert. of Engineering Practice Bachelor of Eng. - Bachelor of Arts (International Studies) Diploma of Eng. Practice
<b>Teaching Unit:</b>	Engineering
<b>Credit Points:</b>	6
<b>Pre-requisite Subject:</b>	48441 Introductory Digital Systems
<b>Co-Requisite Subjects:</b>	
<b>Modes of Presentation:</b>	Weekly classes and tutorials
<b>Current coordinator:</b>	Dr. KK Fung

### Objectives:

The objectives of this subject are that students should learn to analyse, design and implement a programmable digital system based on a user requirement specification, and to understand advanced microprocessor and microcomputer architectures.

### Content and Method:

The subject provides an in depth understanding of the analysis, design and implementation of digital hardware at medium scale computer system building block level. It builds on the basics of Introductory Digital Systems introduced in the earlier "field of practice" subjects. This subject Advanced Digital Systems is compulsory to the Electrical and Computer Systems Engineering degree students.

The subject has five major components:

- (1) Review of basic digital techniques and their application to the design of state machines used in control units.
- (2) Digital hardware design process and Programmable Logic
- (3) VHDL
- (4) Computing technologies
- (5) Microprocessor and Microcomputer architectures

Topics covered include:

Logic fundamentals: Review of combinational and sequential logic circuits, Karnaugh maps; sequential logic design using state tables, state diagrams, excitation table; counters, shift registers; analysis and design procedures; implementation technologies, ASIC and USIC, PLD (Programmable Logic Devices), VHDL (Very high speed integrated circuit Hardware Description Language) specification, synthesis and simulation; CISC and RISC computer architectures, memory and I/O sub-systems.

### Assessment:

<b>Assignment 1</b>	<b>10%</b>	<b>Introductory VHDL</b>
<b>Assignment 2</b>	<b>10%</b>	<b>VHDL application 1</b>
<b>Assignment 3</b>	<b>10%</b>	<b>VHDL application 2</b>
<b>Quiz 1</b>	<b>30%</b>	
<b>Quiz 2</b>	<b>40%</b>	

To pass the subject, you are required to *pass the two quizzes* in total, i.e. obtain at least 35 out of 70 marks, and have an overall mark above 50.

You are strongly advised not to miss quiz 1 and 2 because alternate examinations to be offered later are significantly harder.

*Watch out for the Further Action Required (FAR) list in the UPO at the end of the semester for offer(s) of alternate and supplementary examination, as you will not be notified by any other means.*

**Text:**

Mano MM, Kime CR, "Logic and Computer Design Fundamentals", 3rd edition, Prentice Hall, 2004

Andrew Rushton, "VHDL for Logic Synthesis", 2<sup>nd</sup> edition, John Wiley and Sons

**References**

Wakeley John F., "Digital Design Principles and Practices", 3<sup>rd</sup> edition, Prentice Hall, 2000

Yalamanchili S, "VHDL Starter's Guide", Prentice Hall, 1998

Pellerin D, Taylor D, "VHDL Made Easy!", Prentice Hall PTR, 1997

Zwolinski, Mark, "Digital Systems Design with VHDL", Prentice Hall, 2000

Hennessy JL, Patterson DA, "Computer Architecture a Quantitative Approach", Morgan Kaufmann Publishers, Inc., 1990

**Subject Administration:**

Staff:

Subject coordinator and lecturer: KK Fung  
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Tutorials are staggered one week behind the lectures. Each tutorial is made up of a number of questions and one or more reading paper(s). These serve to reinforce and expand on materials covered in lectures; hence some questions may go beyond the lecture material. Solutions to most questions are provided. During tutorial classes, your tutor will only answer questions. It is therefore important that you attempt all tutorial questions before attending your tutorials. You only come to tutorials to ask questions on parts that you do not understand, or to join in some discussions on the readings.

Laboratories are Operating Systems Lab (Room 1/2214), Microcomputer Lab (Room 1/2318) and Engineering Lab 2/648. Register in this class by filling up the class list on your first lecture will ensure your pin access to these laboratories. However, if you never have a PIN before (eg. this is your first semester in UTS), fill up a Laboratory Access application form obtainable from UPO. Have it signed by all relevant people, then take it to Security on level 4 to apply for a new pin. Similarly procedure to follow if you have forgotten your PIN, or it simply refuses to work.

While attendance in lectures or tutorials is not compulsory, roll calls will be taken in all classes and recorded. If you do not come to classes without a proper reason, please do not expect teaching staff to answer your questions later, or help you with problems that have already been discussed.

Emails accepted, response within 3 days. However, you are strongly encouraged to use the Discussion Board inside UtsOnline for any questions regarding the subject material, and reserve email only for personal matters. You have a better chance of getting your questions answered quickly on UtsOnline Discussion Board, either by fellow students, tutors or myself. This has proven to be very effective in the past semesters.

**Weekly Schedule 2004 Autumn**

<b>Week starting</b>	<b>Lecture: Friday evening</b>	<b>Tutorial: Monday evening</b>	<b>Assignment</b>
1 (1/3/04)	Lecture 1: Subject fundamentals	None	
2 (8/3/04)	Lecture 2: Programmable Logic Devices	Tutorial 1	
3 (15/3/04)	Lecture 3: VHDL	Tutorial 2	Assignment 1 handout
4 (22/3/04)	Lecture 4: VHDL	Tutorial 3/Lab	
5 (29/3/04)	Lecture 5: VHDL	Tutorial 4/Lab	
6 (5/4/04)	Good Friday	Tutorial 5/Lab	Assignment 1 due/ Assignment 2 handout
(12/4/04)	<b>Vice-Chancellor's Week</b>		
7 (19/4/04)	<b>Tutorial Week</b>	<b>Quiz 1</b>	
8 (26/4/04)	Lecture 6: Digital circuit design process and Computer systems architectures	Anzac Day	
9 (3/5/04)	Lecture 7: Central processing units	Assignment 2 demonstration	Assignment 2 due/ Assignment 3 handout
10 (10/5/04)	Lecture 8: Memory	Tutorial 6 & 7	
11 (17/5/04)	Lecture 9: Interfacing techniques	Tutorial 8 & 9	
12 (24/5/04)	Lecture 10: Advanced computer architectures	Assignment 3 demonstration	Assignment 3 due
13 (31/5/04)	Lecture 11: Advanced computer architectures	Tutorial 10 & 11	
14 (7/6/04)	Revision	<b>Quiz 2</b>	
(14/6/04)	<b>Exam Periods</b>		
(21/6/04)			
(28/6/04)			

\* Assignment is due at the time your tutorial starts. Please submit to tutors who are also responsible for marking them.

\*\* It is strongly recommended that you make sure your cpld board is soldered and fully tested at least one week before assignment 2 is due.